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**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Sheet 1 of 1

## Complete if Known

Application Number 09/893,868

Filing Date June 29, 2001

First Named Inventor FLETCHER, Thomas

Group Art Unit 2819

Examiner Name Not assigned

Attorney Docket Number 2207/11272

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## U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code <sup>2</sup> (if known)			
LC		6,208,907 B1	03/27/2002	DURHAM et al	
1/17/08					

## FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD- YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup> - Number <sup>4</sup> - Kind Code <sup>5</sup> (if known)				

## OTHER PRIOR ART -- NON-PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
LC		Yee et al, "Clock-Delayed Domino for Dynamic Circuit Design", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 8, No. 4, August 2000, pp 425-430	
LC		Yee et al, "Clock-Delayed Domino for Adder and Combinational Logic Design", IEEE, 1063-6404/96, pp 332-337, 1996	
LC		Jung, Perepelitsa, Sobelman, "Time Borrowing in High-Speed Functional Units Using Skew-Tolerant Domino Circuits," Proceedings, IEEE International Symposium on Circuits and Systems, pp. V-641 - V-644, 2000	
LC		Presentation by Carl Sechen dated March 17, 2000.	
LC		Taub, <i>Digital Circuits and Microprocessors</i> , pages 205-212, McGraw-Hill, 1982	

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